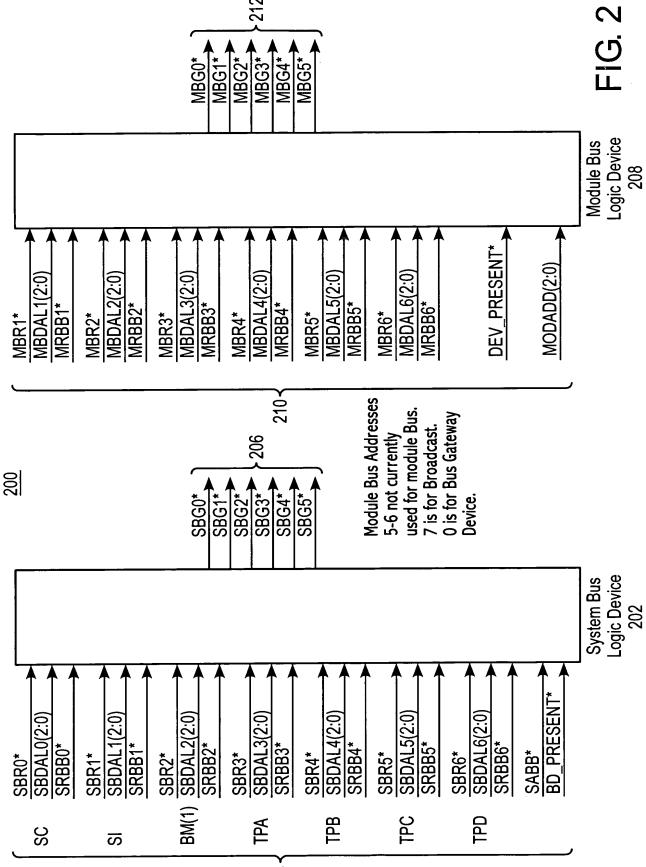
APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. No.: 09/955,961
SHEET **SHEET 1 OF 13** 128 124 126 122 DAdd=3 PPC-C MEM BUSI Temporal Processor Module C Module Bus 102 126 8 124 2 BAdd Config Module Add = 5 DAdd=2 PPC-B MEM BUSI 130 2 126 82 36 134 BUS Gateway DAdd=0 BUS IFC DAdd=1 PPC-A MEM Private Memory DMA Memory Sensor Interface 132 38 126 **5**8 124 122 BUS IFC DAdd=3 116 BUS IFC DAdd=0 PPC-C MEM 240 Temporal Processor Module B Module Bus 124 1281 <u>|</u>26 BAdd Config Module Add = 4 Bus Addr Mod Add=1 **BUS IFC** DAdd=2 PPC-B MEM 120 126 128 BUS Gateway DAdd=0 **BUS IFC** DAdd=1 PPC-A MEM+ System Bus 5 Mod Add=0 SBR* (7:0) **Bus Addr** 126 128 SBG*(7:0) 124 122 BUS IFC DAdd=3 114 PPC-C MEM Temporal Processor Module A Module Bus System Controller 9 8 1281 BAdd Config Module Add = 3 126 124 DAdd=0 MEM **Arbitration Unit** BUS IFC DAdd=2 BUSI System Bus PPC-B MEM <u>| 50</u> <u>|</u> PPC-A |24 106 BUS Gateway DAdd=0 BUS IFC DAdd=1 PPC-A MEM+ 8

APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. No.: 09/955,961 SHEET 2 OF 13



TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS INVENTOR(S): GREGORY S. ANDRE APPLN. NO.: 09/955,961 SHEET **SHEET 3 OF 13** 366 Module 0 오 358 回 FIG. 3 348 362 360 Module 1 외 338 346 **Bus Chip Buffer)** D ID HO DO D1 D2 SC Requests Bus for Write Burst (Fills TPA 332 Module 0 11328 Address Data 342 326 306 - SBDALO 322 \ SDBB* | 308 ~ SRBB0* 310 \ SRBB1* 316 ~ SBG1* 302 \sim CLK -312 \ SBG0*_ $320 \sim SABB^*$ 314 \ SBR1* 304 \ SBR0*

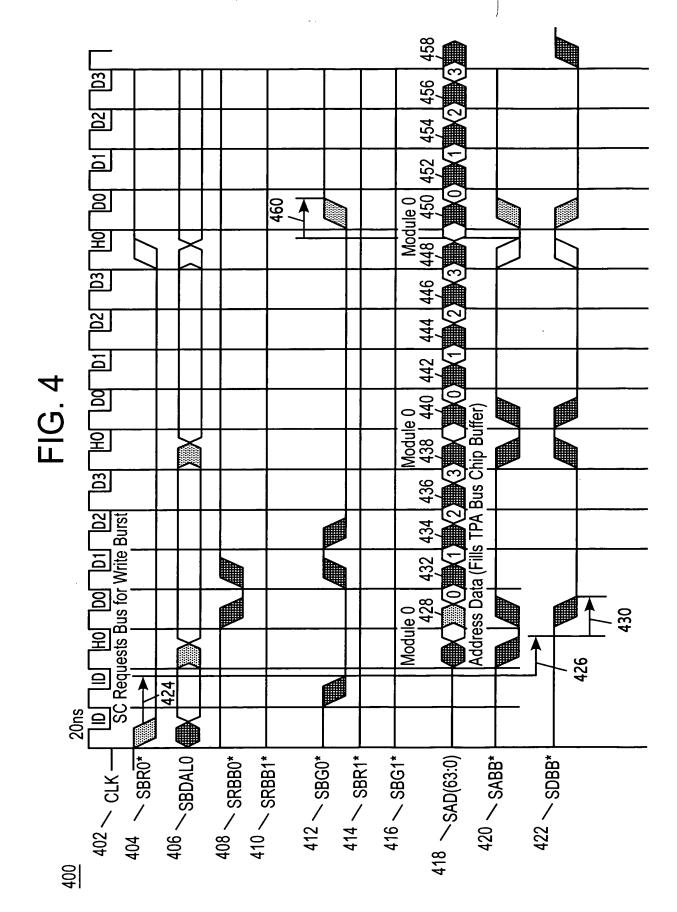
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APPLN. FILING DATE: SEPTEMBER 20, 2001

APPLN. FILING DATE: SEPTEMBER 20, 2001 TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS

INVENTOR(S): GREGORY S. ANDRE APPLN. NO.: 09/955,961

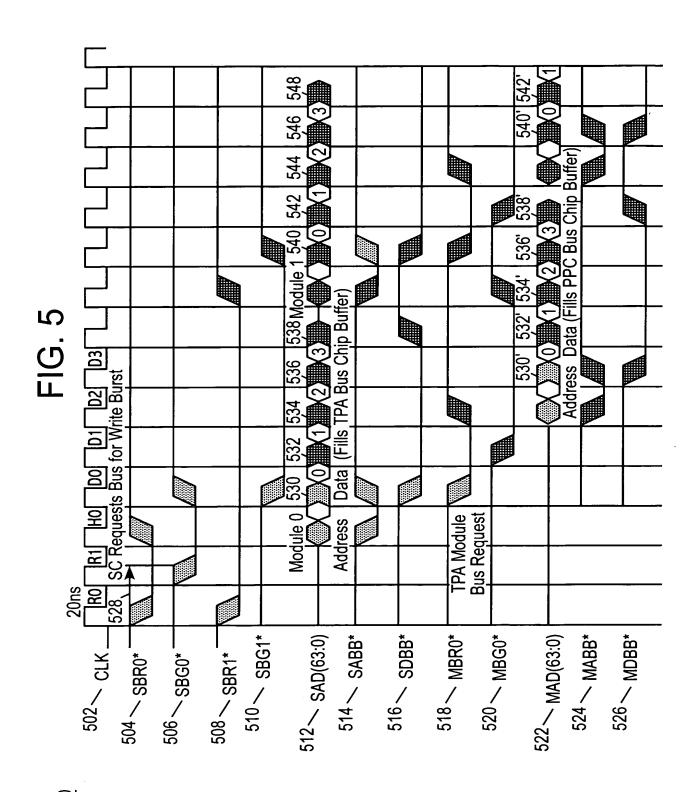
SHEET 4 OF 13



APPLN. FILING DATE: SEPTEMBER 20, 2001 TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS

Inventor(s): Gregory S. Andre Appln. No.: 09/955,961

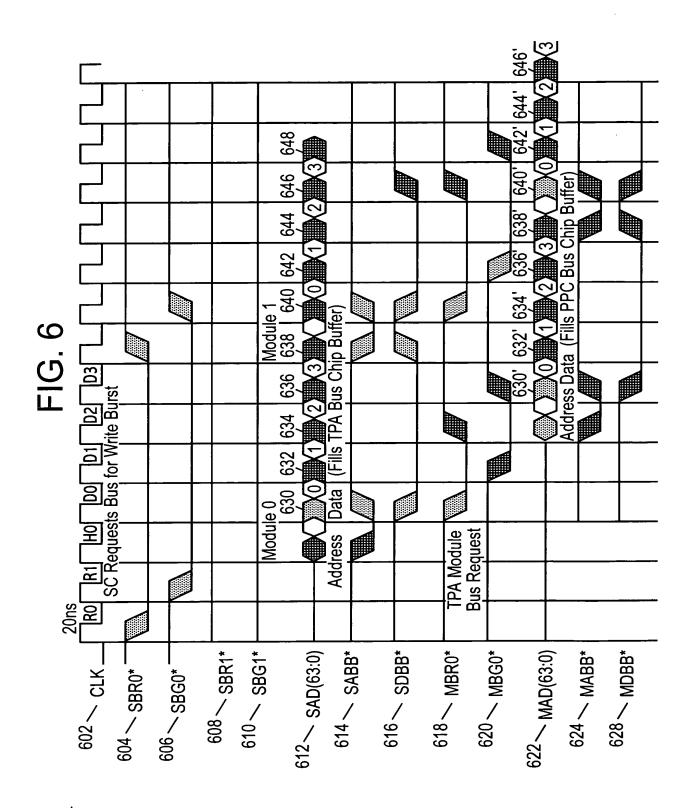
SHEET 5 OF 13



APPLN. FILING DATE: SEPTEMBER 20, 2001 TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS

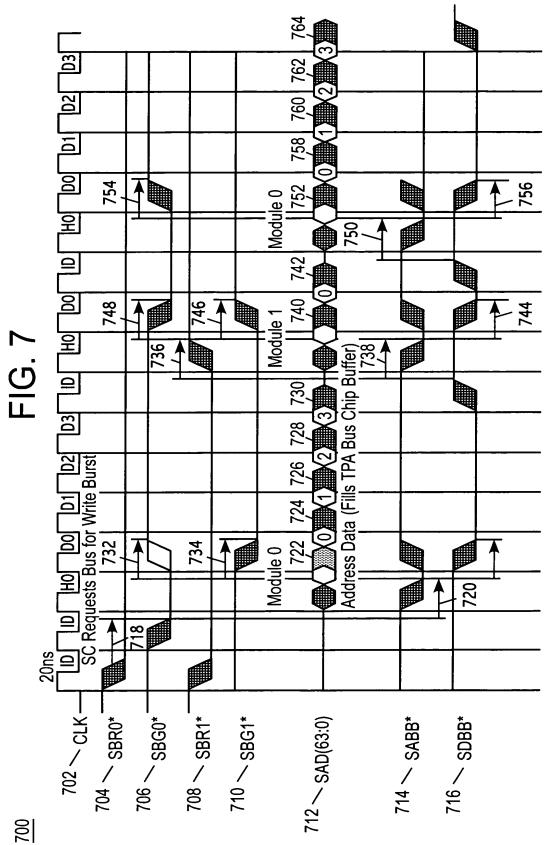
Inventor(s): Gregory S. Andre APPLN. No.: 09/955,961

SHEET 6 OF 13



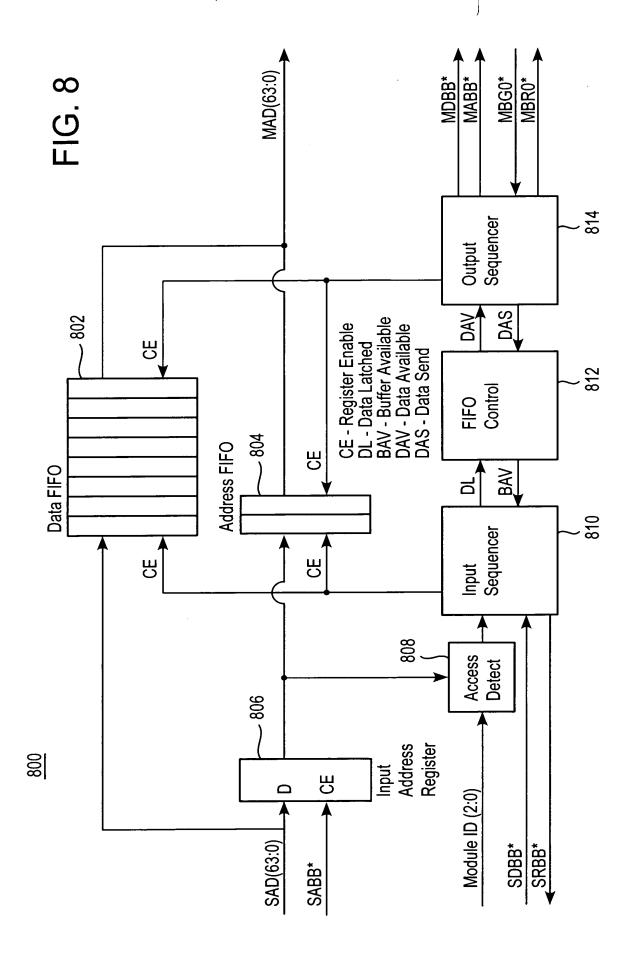
APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. No.: 09/955,961
SHEET

SHEET 7 OF 13



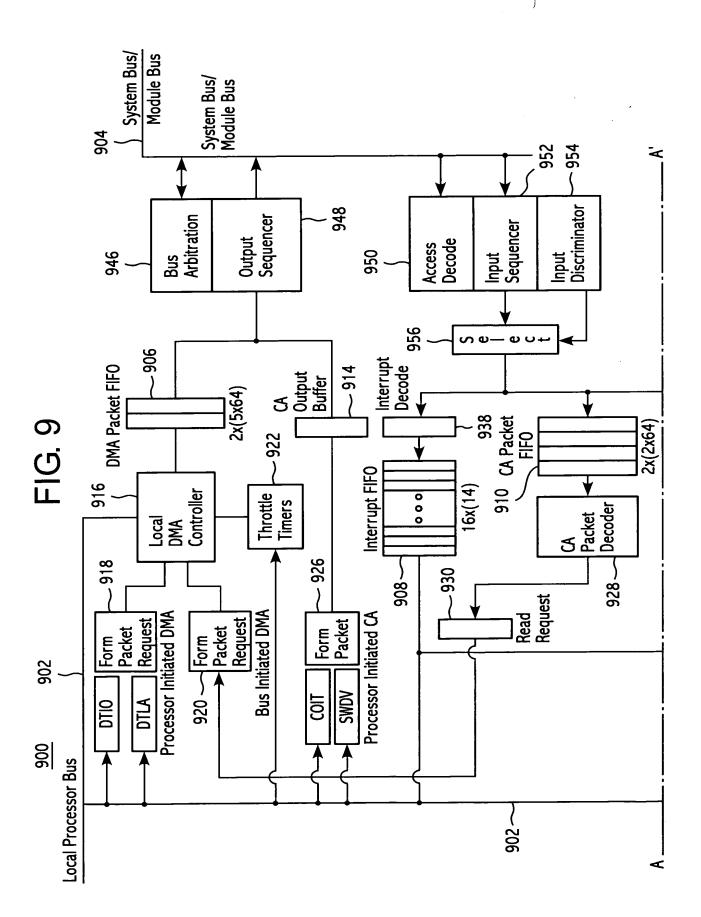
APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. NO.: 09/955,961
SHEET

SHEET 8 OF 13



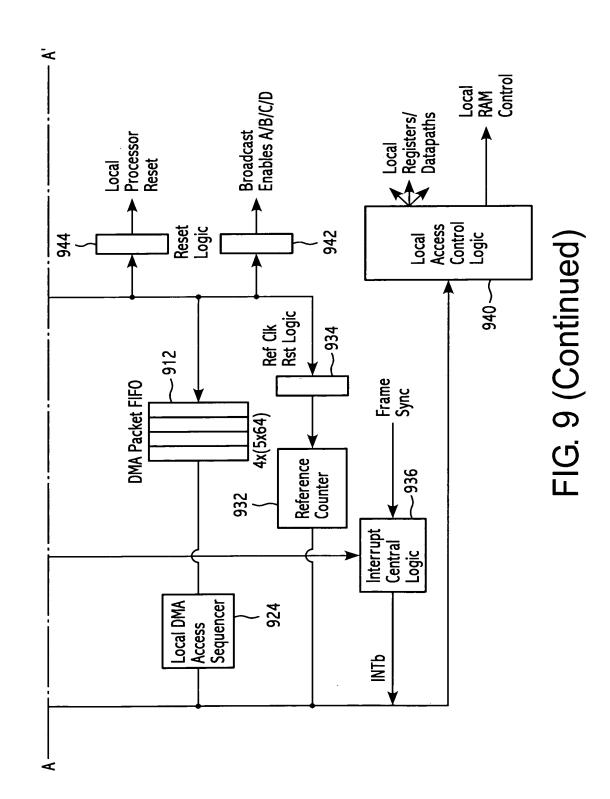
APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. NO.: 09/955,961
SHEET

SHEET 9 OF 13



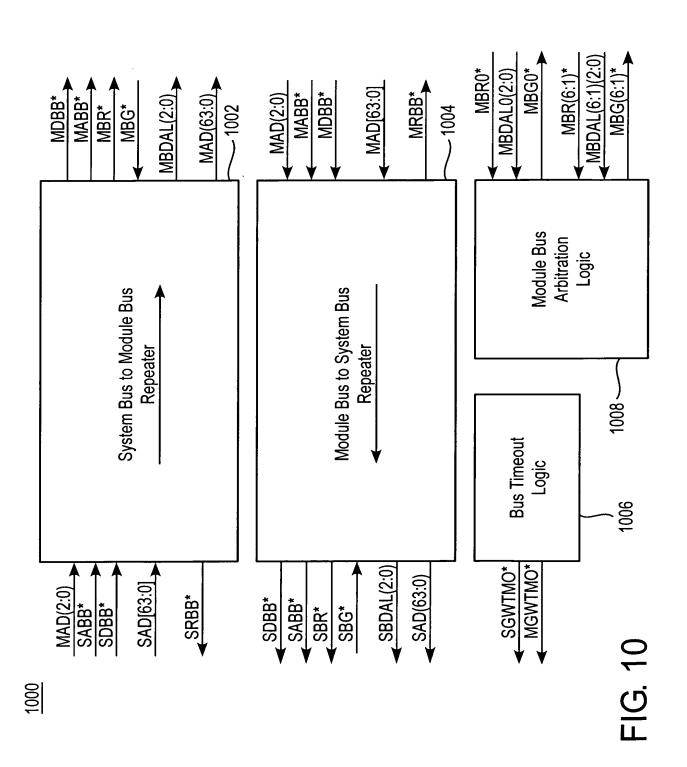
APPLN. FILING DATE: SEPTEMBER 20, 2001 TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS INVENTOR(S): GREGORY S. ANDRE APPLN. NO.: 09/955,961 SHEET

SHEET 10 OF 13



APPLN. FILING DATE: SEPTEMBER 20, 2001
TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS
INVENTOR(S): GREGORY S. ANDRE
APPLN. No.: 09/955,961
SHEET

SHEET 11 OF 13



APPLN. FILING DATE: SEPTEMBER 20, 2001 TITLE: TWO LEVEL MULTI-TIER SYSTEM BUS INVENTOR(S): GREGORY S. ANDRE APPLN. NO.: 09/955,961 SHEET **SHEET 12 OF 13** MDBB* **MBDAL**(2:0) MABB* MBR* MAD(63:0) **MBG*** Output Sequencer Output Buffer 1118 1112 Packet Buffer (64x5x1) 1116 Output Mux 1110 Main Buffer (64x5x4) Circular Buffer Control 1104 Discriminator Packet Buffer (64x5x1) Sequencer Input 1102 മ FIG. 11 Input Buffer ェ 1100 SAD[63:0] SABB* SRBB*

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APPLN. NO.: 09/955,961
SHEET

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